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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/785,073	02/25/2004	Teruo Takizawa	118439	8936

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EXAMINER	
QUINTO, KEVIN V	
ART UNIT	PAPER NUMBER
2826	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	01/25/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/785,073	TAKIZAWA, TERUO	
	Examiner	Art Unit	
	Kevin Quinto	2826	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *27 October 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,2,4,5 and 8* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,2,4 and 5* is/are rejected.

7)☒ Claim(s) *8* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

1. Applicant's arguments with respect to claims 1, 2, 4, 5, and 8 have been considered but are moot in view of the new ground(s) of rejection.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 1, 4, and 5 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hayashi (United States Patent Application No. US 2003/0197598 A1) in view of Adkisson et al. (United States Patent Application Publication No. US 2003/0059985 A1) and further in view of Huang (United States Patent Application Publication No. US 2003/0102534 A1) and further in view of DiBuganara (USPN 4,126,713).

4. With regard to claims 1 and 4, Hayashi (United States Patent Application No. US 2003/0197598 A1) discloses a similar device. Figures 9 and 10 of Hayashi disclose a semiconductor device with a bridge rectifier circuit (3 in figure 9, figure 10 has added detail) having a plurality of diodes (D1-D4, figure 10) which rectify a predetermined alternating-current voltage to a direct-current voltage. Hayashi does not disclose the use of a diode formed on an insulating substrate having using a p-type silicon layer and

an n-type silicon layer. However the use of such diodes is well known in the art. Adkisson et al. (United States Patent Application Publication No. US 2003/0059985 A1, hereinafter referred to as the "Adkisson" reference) discloses such a diode. In figures 11 and 13 of Adkisson, there is a p-type silicon layer (180 or 220) joined to an n-type silicon layer (185) which are both disposed on the insulating substrate (270). The p-type silicon layer (180 or 220) is surrounded by the n-type silicon layer (185). Adkisson makes it clear that the diode of figures 11 and 13 has the benefit of a larger breakdown voltage compared to that of a CMOS device gate dielectric (p. 1, paragraph 5). Adkisson makes it clear that semiconductor devices with large breakdown voltages are a known goal in the semiconductor art (p. 1, paragraph 4). In view of Adkisson, it would therefore be obvious to implement the Adkisson diode in the bridge rectifier circuit of Hayashi. Adkisson does not disclose using p-type silicon with germanium for the anode of the diode. However the use of such materials in a diode is well known in the art. Huang (United States Patent Application Publication No. US 2003/0102534 A1) discloses that the use of p-type silicon with germanium for the anode in a diode gives it the benefit of a reduced reverse recovery time (p. 1, paragraphs 10-11). DiBuganara (USPN 4,126,713) discloses that the reduction of reverse recovery time in diodes is a known goal in the art (column 1, lines 16-25). In view of Huang and DiBuganara, it would therefore be obvious to use p-type silicon with germanium as the anode in the diode of Adkisson.

5. With regard to claim 5, figure 9 of Hayashi shows that the semiconductor device has a coil antenna (L1) coupled to one side of the bridge rectifier circuit (3); a smoothing

capacitor (Ca) coupled to the other side of the bridge rectifier circuit (3). The coil antenna (L1) generates an alternating-current voltage by electromagnetic induction. The bridge rectifier circuit (3) rectifies the alternating-current voltage into a direct-current voltage. The smoothing capacitor (Ca) smoothes the direct-current voltage into a constant voltage.

6. Claim 2 is rejected under 35 U.S.C. 103(a) as being unpatentable over Matsushita (USPN 3,710,206) in view of Huang (United States Patent Application Publication No. US 2003/0102534 A1) and further in view of DiBuganara (USPN 4,126,713).

7. In reference to claim 2, Matsushita (USPN 3,710,206) discloses a device which meets the claim. Figures 8 and 9 of Matsushita disclose a PIN diode on an insulating substrate (14, 12). There is a p-type silicon layer (D3) which is joined to an intrinsic silicon layer (π). An n-type silicon layer (D2) is joined to the intrinsic silicon layer (π). The p-type silicon layer (D3), intrinsic silicon layer (π), and the n-type silicon layer (D2) are all disposed on the insulating substrate (92). The intrinsic silicon layer (π) is surrounded by the n-type silicon layer (d2). The p-type silicon layer (D3) is surrounded by the intrinsic silicon layer (π). Matsushita does not disclose using p-type silicon with germanium for the anode of the diode. However the use of such materials in a diode is well known in the art. Huang (United States Patent Application Publication No. US 2003/0102534 A1) discloses that the use of p-type silicon with germanium for the anode in a diode gives it the benefit of a reduced reverse recovery time (p. 1, paragraphs 10-11). DiBuganara (USPN 4,126,713) discloses that the reduction of reverse recovery

time in diodes is a known goal in the art (column 1, lines 16-25). In view of Huang and DiBuganara, it would therefore be obvious to use p-type silicon with germanium as the anode in the diode of Matsushita.

8. Claim 2 is rejected under 35 U.S.C. 103(a) as being unpatentable over Poveda (United States Patent Application Publication No. US 2004/0135235 A1) in view of Huang (United States Patent Application Publication No. US 2003/0102534 A1) and further in view of DiBuganara (USPN 4,126,713).

9. In reference to claim 2, Poveda (United States Patent Application Publication No. US 2004/0135235 A1) discloses a device which meets the claim. Figures 2 and 3 of Poveda disclose a PIN diode on an insulating substrate (32). There is a p-type silicon layer (41 or 43 or 50 or 55) which is joined to an intrinsic silicon layer (42 or 44 or 51 or 56). An n-type silicon layer (40) is joined to the intrinsic silicon layer (42 or 44 or 51 or 56). The p-type silicon layer (41 or 43 or 50 or 55), intrinsic silicon layer (42 or 44 or 51 or 56)), and the n-type silicon layer (40) are all disposed on the insulating substrate (32). The intrinsic silicon layer (42 or 44 or 51 or 56) is surrounded by the n-type silicon layer (40). The p-type silicon layer (41 or 43 or 50 or 55) is surrounded by the intrinsic silicon layer (42 or 44 or 51 or 56). Poveda does not disclose using p-type silicon with germanium for the anode of the diode. However the use of such materials in a diode is well known in the art. Huang (United States Patent Application Publication No. US 2003/0102534 A1) discloses that the use of p-type silicon with germanium for the anode in a diode gives it the benefit of a reduced reverse recovery time (p. 1, paragraphs 10-11). DiBuganara (USPN 4,126,713) discloses that the reduction of reverse recovery

time in diodes is a known goal in the art (column 1, lines 16-25). In view of Huang and DiBuganara, it would therefore be obvious to use p-type silicon with germanium as the anode in the diode of Poveda.

Allowable Subject Matter

10. Claim 8 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

11. The following is a statement of reasons for the indication of allowable subject matter: the examiner is unaware of any prior art which suggests or renders obvious a bridge rectifier circuit containing the explicit PIN diode structure suggested by the applicant.

Conclusion

12. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the

shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Kevin Quinto whose telephone number is (571) 272-1920. The examiner can normally be reached on M-F 8AM-5PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Sue Purvis can be reached on (571) 272-1236. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

KVQ

LEONARDO ANDUJAR
PRIMARY EXAMINER